



In re application of:

Sharad Kapur, *et al.*

2123  
41  
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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JUN 17 2004

Serial No.: 09/427,238

Technology Center 2100

Filed: October 26, 1999

For: SYSTEM AND METHOD FOR DETERMINING CAPACITANCE  
FOR LARGE-SCALE INTEGRATED CIRCUITS

Group No.: 2123

Examiner: Eduardo Garcia-Otero

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

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Sharadine Pitt  
(Signature of the person signing the certificate)

Sir:

AMENDMENT UNDER 37 C.F.R. § 1.111

The Applicants have carefully considered this application in connection with the Examiner's Action mailed on March 10, 2004, and respectfully request reconsideration of this application in view of the following amendment and remarks.